RPW Instrument

BIAS Specification

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Change Record

Issue	Rev.	Date	Authors	Modifications
1	0	2011.01.21	Team	Initial version
1	1	2011.02.08	Team	Initial version
1	2	2011.09.30	A.Vaivads, S-E Jansson	Updated table on BIAS output signals, added serial link
1	3	2011.12.19	Team	Updated document
1	5	2012.02.21	A.Vaivads, L Ahlen.	Update of 1.7 to 3.8
1	6	2012.01.17	L Ahlen	3.5 Power interface requirements
1	7	2012.01.21	W Puccio	Serial link, memory map & registers
1	8	2012.01.31	W Puccio	Corrected typo in 2.4.1.10 added description of internal sweep mode
1	9	2013.05.24	L Åhlen W Puccio	Update Thermal, Mass, power, Main block diagram and MUX layout. Mux has more bits, differential signal 1&2/1&3 (2.4.2.4-6 & 2.4.4.14). REF now measures GND(10bit)&1.5V(6bit) (2.4.4.7)
1	10	2013.10.02	Team	Update based on MEB PM and Stellar report
1	11	2013.11.07	Team	Updated functional and operational requirements plus some minor fixes.
1	12	2014.04.16	V Cripps	*Introduction* numbering corrected, now Section 2. *Communication Interface Requirements* numbering corrected, now Section 5. All other numbering updated accordingly. Figures 4, 6, 7 updated. Corrected Table 6 (SET_RELAY, bits 6 & 7 inverted). DC/DC converter interface figure in Section 4.5 (was 3.5) now numbered, now Figure 11. All other figure numbers updated accordingly. 5.2.2 (was 3.9.2) *Serial link front plug (equipment side)* figure and table updated. *Serial link front plug (DPU side),* including figure, deleted. Section 1.4 Responsibilities updated. Table 4 updated to clarify V12_AC*. Relay switch position corrected in Figure 7. General reformatting and corrections.
1	13	2014.04.23	V. Cripps	Reference documents RD4 to RD9 added. Removal of text, figures and tables and improved cross-referencing, to avoid duplication of information in several documents. Changes as follows: - Fig. 4, 7. 8, 9, 10, 11 deleted, references to RD4 + 5 added - Tables 6 and 7 deleted, references to RD4. 1.4 Responsibilities updated. 2.3.1 Table 2 updated. 2.3.2.1 Ref to Fig. 5 corrected to Fig. 6. 2.3.2.4 100x gain added and text updated.

				3.4.1 32bit removed. 3.4.6 REQ-RPW-BIA-2403 + 4 updated to refer to FPGA Plan Memory Map, Table 1 [RD4]. 2.3.2.9 and 5.4.1 Ref to RD6 added. 4.6.1 and 4.6.1.1 updated. 4.6.1.2 added. 4.6.2.2 updated for gain 100.
1	14	2014.05.08	V. Cripps	Section 3.1. REQ-RPW-MEB-0102 updated to ±60µA. New section 3.1.1 and updates to REQ-RPW-MEB-2101, REQ-RPW-MEB-2102, REQ-RPW-MEB-2103 and REQ-RPW-MEB-2104. Section 3.2 Update to REQ-RPW-MEB-2202. AD1 updated to i3.0 dated 2014/04/28.

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1 GENERAL

1.1 Scope of the Document

The purpose of this document is to define the functional and interface requirements of the BIAS unit. This document shall be used as an internal reference document within the RPW and will be used as an applicable document.

1.2 Applicable Documents

This document responds to the requirements of the documents listed in the following table:

Mark	Reference	Title of the document	Authors	Date
AD1	RPW-SYS-MEB-SPC-00021-LES_Iss03Rev00	Specification for the Main Electronics Box	M. Dekkali	2014/04/28

According to [AD1] BIAS unit shall satisfy Requirements from REQ-RPW-MEB-0101 up to REQ-RPW-MEB-0108.

1.3 Reference Documents

This document is based on the documents listed in the following table:

Mark	Reference	Title of the document	Authors	Date
RD1	SOL-EST-RCD-0050-Issue2-Rev8	SO Experiment Interface Document – Part A	Solar Orbiter project	2011/10/14
RD2	SOL-RPW-EID– Issue2 – Rev1	RPW Experiment Interface Document – Part B	RPW Team	2010/04/09
RD3	RPW-SYS-SRD-00040-Issue1-Rev2	RPW Science Requirements	RPW Team	2012/02/29
RD4	RPW-SYS-MEB-BIA-PLN-00041-IRF Iss01_Rev01	FPGA Development Plan	W. Puccio	2014/04/16
RD5	RPW-SYS-MEB-BIA-DRP-00013_IRF Iss01_Rev04	BIAS Design Description	V. Cripps	2014/04/30
RD6	RPW-SYS-MEB-DPH-TN-00022-IWF DPU PDU Bias Protocol	RPW DPU Technical Note – DPU-PDU/BIAS Protocol	IWF team	2014/05/24
RD7	RPW-SYS-MEB-BIA-UMA-00037-IRF Iss01_Rev03	BIAS User Manual	V. Cripps	2014/04/16
RD8	RPW-SYS-ELE-ICD-00034-LES Iss04_Rev03	RPW Electrical Interface Control Document	MEB team	2013/10/01
RD9	RPW-SYS-MEB-BIA-ICD-00022-IRF Iss01_Rev04	BIAS Interface Control Document	V. Cripps	2014/05/08

According to [RD3] BIAS unit shall satisfy following Requirements (in parenthesis are given page numbers where compliance with the requirements is discussed):

REQ-RPW- SCI-0002 (p.9), REQ-RPW- SCI-0003 (p.12), REQ-RPW- SCI-0004 (p.12), REQ-RPW- SCI-0005 (p.12), REQ-RPW- SCI-0006 (p.12).

1.4 Responsibilities

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2 INTRODUCTION

2.1 Equipment Overview

The basic principle underlying DC double-probe measurements is identical to that of a voltmeter: one measures the potential difference between two antennas (probes) which are anchored to the local plasma potential at two positions separated by as large a distance as feasible. Solar Orbiter employs three antennas and there are three possible ways electric field can be determined as the voltage difference between two antennas divided by the effective separation distance between those antennas.

The floating potential V of a conductive surface in a plasma (either an individual probe or the entire spacecraft) is determined by current balance between the outflowing photoelectron current $I_{ph}(V)$ and the inflowing thermal electron current from the plasma $-I_e(V)$. In the expected solar wind plasma parameter range (n=1-500 /cc) [RD3], an illuminated and conductive surface will most of the time charge up positively, attracting back more of its photoelectrons and attracting more ambient electrons until the potential V where $I_{ph}(V) + I_e(V) = 0$. In this case, the floating potential will depend on the density and (to a lesser extent) the temperature of the surrounding electrons through the current $I_e(V)$. This effect can be used to determine the plasma density by measuring the floating potential of the entire spacecraft.

In contrast to the spacecraft potential, the probe potential should be anchored tightly to the local plasma potential, and should not depend on the plasma parameters. To achieve this, we draw a constant bias current I_b from the probes to the spacecraft. If the bias current is suitably chosen [$I_b \sim -(0.5\text{-}0.7)I_{ph}(V=0)$] , then the current balance equation $I_{ph}(V) + I_e(V) + I_b = 0$ is

satisfied at a relatively small voltage V (~1V), so that the probes float close to the local plasma potential. At these small voltages, $I_e(V) \sim 0$, so that the probe potential is not a function of the plasma parameters. Moreover, $I_{ph}(V)$ is strongly dependent on V (i.e. the probe-plasma resistance dV/dI is small), so that the voltage is relatively insensitive to stray currents.

2.2 Scientific Objectives and Performances

2.2.1 Motivation for Biased Electric Antennas

The main motivation to have electric antennas biased by a current are [RD3]:

Reliable DC/LF measurements of electric field E. By adjusting a bias current it is possible to anchor the electric antennas very close to the local plasma potential. This gives the lowest values of antenna-plasma resistance that significantly improves the measurement quality and the signal-to-noise ratio.

Capability to estimate satellite potential and derived plasma density. The potential of the biased antenna is very close to the plasma potential and thus the potential difference between the antenna and spacecraft gives a good estimate of the spacecraft potential. The floating potential of the (unbiased) spacecraft is mainly a function of plasma density. Hence, the antenna-spacecraft potential can be used for plasma density estimates on a fast temporal scale. This would allow the measurement of plasma density fluctuations with temporal resolution up to a few kHz, covering characteristic ion and electron scales. In addition, knowledge of the spacecraft potential significantly improves the analysis of electron instrument data at the lowest energies.

Capability to estimate integrated UV emission from the Sun. Photoelectron current is a function of the solar UV emission. The possibility exists to make current/voltage sweeps of antennas at regular intervals. This would allow estimation of photoelectron current and thus monitoring of the solar UV emission throughout the mission.

2.2.2 Antenna Potential and Resistance

The local potential at the probe position is affected by the nearby presence of the positively-charged spacecraft. Accurate measurement of the ambient DC electric field requires rejecting this common potential on the two probes. Simulations show that the local potential shift near the antennas due to the spacecraft is about 20% of the spacecraft potential, which is similar to the effect seen on previous magnetospheric missions such as Cluster and THEMIS.

As discussed above, the spacecraft potential depends on the plasma density and electron temperature. Figure 1 shows the antenna IU curve and antenna plasma resistance values calculated for typical plasma parameters at two distances from Sun roughly corresponding to the aphelion and perihelion of Solar Orbiter during its science phase. One can see that a biased antenna has its potential close to the plasma potential. Measuring the potential difference between the biased antenna and satellite gives an estimate of the satellite potential satisfying science requirement [RD3] REQ-RPW- SCI-0002.

In the expected density and temperature range, the spacecraft potential is much more dependent on the plasma density than on the electron temperature. Therefore, it can be used to estimate plasma density and density fluctuations. The actual spacecraft potential / density curve can be obtained using in-flight calibration, e.g. using emissions at plasma frequency as

has been done on other spacecraft. The resistance of biased antennas is at least factor 10 lower than for unbiased antennas.

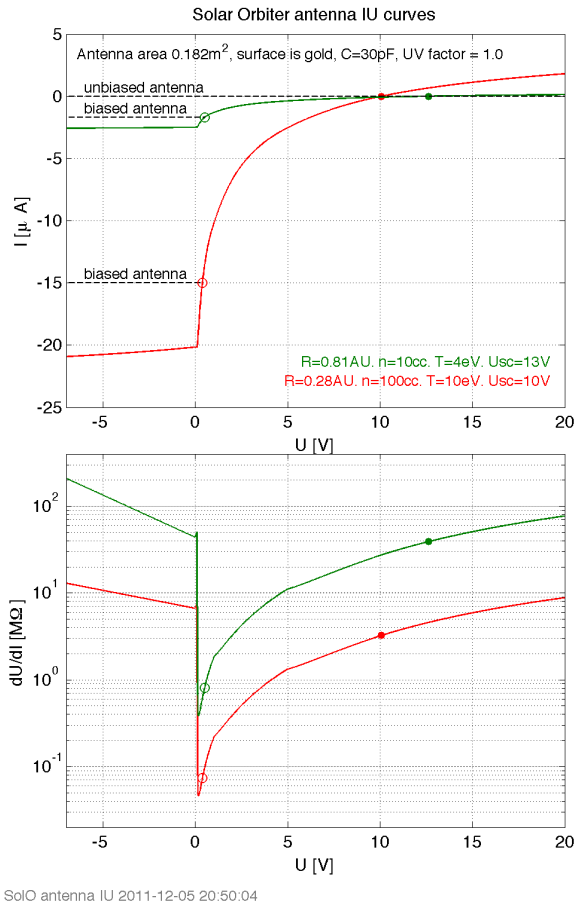

Figure 1 Expected antenna IU curves and resistance.

2.2.3 Antenna Coupling to Plasma.

It is important to estimate at which frequencies spacecraft and antennas are resistively and capacitively coupled to plasma. At low frequencies, when the spacecraft is resistively coupled to plasma, spacecraft potential variations can be directly related to variations in plasma density. At higher frequencies the spacecraft and probes are capacitively coupled to the plasma, and will not vary in phase with density fluctuations (although electric fields still can be accurately measured). Calculated values of capacitance and resistance for the spacecraft and antenna are given in Table 1. The resistance values are taken from numerical estimates for typical solar wind conditions and two different distances from the Sun. The last column shows cross-over frequencies at which coupling changes from being resistive to capacitive. The spacecraft is resistively coupled to plasma up to ~24 kHz at aphelion and 240 kHz at perihelion, while antennas are resistively coupled up to ~ 2 kHz at aphelion and ~20 kHz at perihelion. This means that variation in satellite potential can be used as proxy for density fluctuations at least up to several kHz.

	Capacitance (vacuum)	Resistance	1/(2πRC)
Spacecraft	67 pF	10 kOhm (perih) 100 kOhm (aph)	240 kHz 24 kHz
One antenna	30 pF	100-200 kOhm (perih) 1-2 MOhm (aph)	27-53 kHz 2.7-5.3 kHz

Table 1 Typical values of spacecraft and antenna parameters

2.2.4 Heritage

The proposed instrument has a long heritage, and the performance can be estimated by examining data from existing missions with similar designs. The closest analogy is the axial probe measurements from the Polar and THEMIS spacecrafts. Because they are aligned with spin axis, these measurements are analogous to antennas on a 3-axis stabilized spacecraft. The axial probes on the THEMIS-EFI experiment are about 7m tip to tip and are largely similar in the design to RPW on Solar Orbiter, except that the sensor length on THEMIS is 1m while on Solar Orbiter it would be 5m. The THEMIS sensors are also thinner, and are separated from the spacecraft by a longer boom.

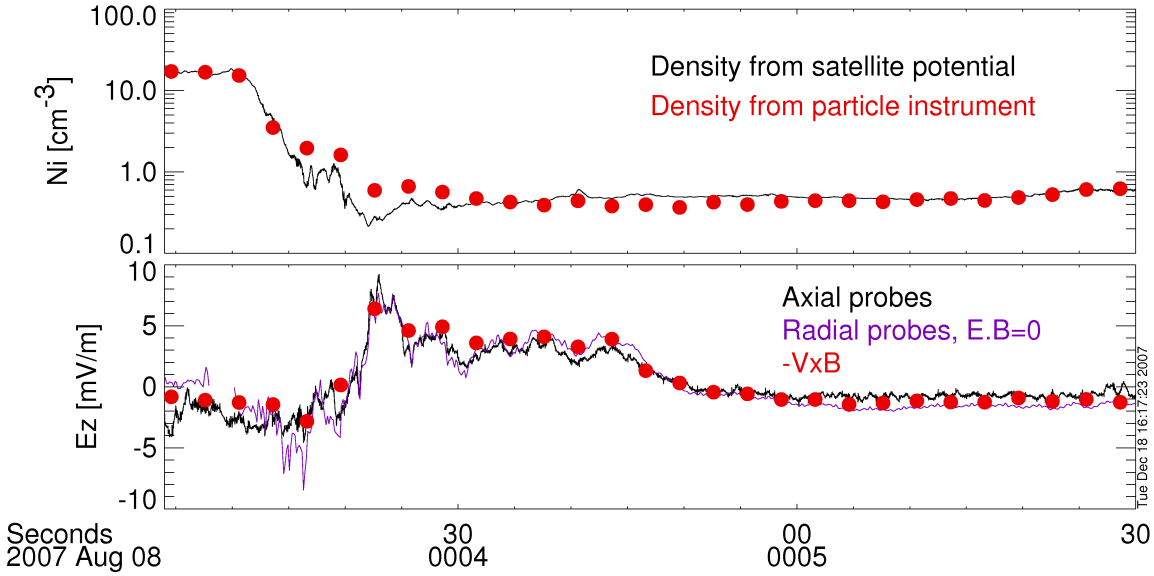

Figure 2 Example of measurements from the axial units of the Themis-EFI experiment.

Figure 2 shows THEMIS data from the axial probes to illustrate the fidelity of the near-DC electric field measurements and density from the spacecraft potential. During the event, THEMIS crosses the magnetopause inbound from the magnetosheath (compressed solar wind) into the magnetosphere. The top panel shows density estimates from the particle instrument and as based on the spacecraft potential. Once the particle instrument data has been used to calibrate the transformation from spacecraft potential to density, the spacecraft potential can be used to follow plasma density variations at very fast time scales. The bottom panel shows electric field measurements from the THEMIS axial probes (black), the electric field expected along the spacecraft spin axis based on measurements from radial probes and the assumption $\mathbf{E}\cdot\mathbf{B}=0$ (blue) and finally the expected electric field estimated from $\mathbf{v} \times \mathbf{B}$ based on particle instrument data (red). While on the large scale the electric field follows the predictions from $\mathbf{v} \times \mathbf{B}$, there are strong localized electric field regions that cannot be resolved by particle instruments and in which the assumption $\mathbf{E} + \mathbf{v} \times \mathbf{B}=0$ may break down. Thus

THEMIS axial probe data shows that we can expect good quality electric field and plasma density fluctuation data from the RPW instrument.

2.3 Instrument Description

2.3.1 Functional Description

Table 2 shows the required and expected performance characteristics of the BIAS unit. Those satisfy requirements from Science Requirement document [RD3] REQ-RPW- SCI-0002 REQ-RPW- SCI-0003, REQ-RPW- SCI-0004, REQ-RPW- SCI-0005, REQ-RPW- SCI-0006.

Quantity	Science requirement	Expected performance	Comments
Floating potential		± 50V	REQ-RPW- SCI-0002 16bit ADC, about 2mV resolution
Electric field	± 500 mV/m	DC ± 1V/m AC ± 200mV/m (gain 5) AC ± 10mV/m (gain 100)	REQ-RPW- SCI-0004, REQ-RPW- SCI-0006
Frequency range	0 – 10kHz	DC 0 – 10 kHz AC 7 Hz – 10 kHz	REQ-RPW- SCI-0004
Resolution	DC 0.1mV/m AC 0.01mV/m	DC 15mV/m AC 3mV/m	REQ-RPW- SCI-0004 Bit resolution (LSB). 16bit ADC
Electronics noise level	10^{-16} $V^2/m^2/Hz$, f > 100 Hz	<10nV/$Hz^{-1/2}$m ~5.10^{-18} $V^2/m^2/Hz$	REQ-RPW- SCI-0005 The frequency at which 1/f-noise starts will be determined by measurement. AC gain 100 is used to achieve the highest sensitivity.
Bias current range		-60µA to +60µA	In 1024 steps

Table 2 The required and expected performance characteristics of BIAS unit. The efficient antenna separation of 6m has been assumed.

There are three main operational modes of the bias circuitry:

2.3.1.1 Fixed Bias

This is the normal operational mode to be used most of the time (99.9% or more). The levels of the bias currents will be fixed separately for each of the probes, the goal being that probes are sitting as close as possible to the plasma potential and at the same time the probe to plasma potential being as equal as possible on all three probes. The bias currents will be held at a fixed level but will be changed to different levels (about once per a few weeks) depending on the spacecraft distance from the sun or depending on the calibration results from the bias sweeps.

2.3.1.2 Bias Sweeps

A bias sweep means stepping through a number of bias settings during a short time to record a current-voltage characteristic (see Figure 1 for typical I-U-curves) of each probe, which is important for instrument diagnostics, for fine–tuning of calibrations of scientific data and for monitoring photoemissions and solar UV flux. Bias sweeps are usually performed on an

hourly to daily basis. A sweep is performed by the DPU. First the DPU sets the "sweep flag" to inform other instruments of the coming sweep. The only instruments that are directly affected by this flag are LFR and/or TDS (in case it samples BIAS outputs). Then the DPU sends the bias setting commands, stepping through the sweep and time tagging the bias setting commands. The implementation of the sweep mode is done in the software: there is no additional hardware involved. The sweep data are collected by LFR and put into the normal telemetry.

Bias sweeps have to be carried out separately on each of the three probes. All three sweeps take approximately 5 minutes. Figure 3 shows voltage-current relationship for two antennas on Solar Orbiter as obtained from numerical simulations of the spacecraft environment. Figure 3 illustrates that if two of the probes are kept at the same bias current then there will be a voltage difference between those probes of the order 0.5V. This is not a real electric field but an offset due to the spacecraft environment. To compensate for this offset it is important to run bias sweeps on all three probes separately and based on the results adjust the bias current values to minimize the offset among the probes. However, it will not be possible to fully compensate in this way for the offset and thus electric field measurements should expect the presence of such a DC offset. Thus if the electric field (analogue difference between the probe signals) is digitized then either the range should be large enough to accommodate the possible presence of DC offset or the signal should be AC-coupled to remove offset before digitalization.

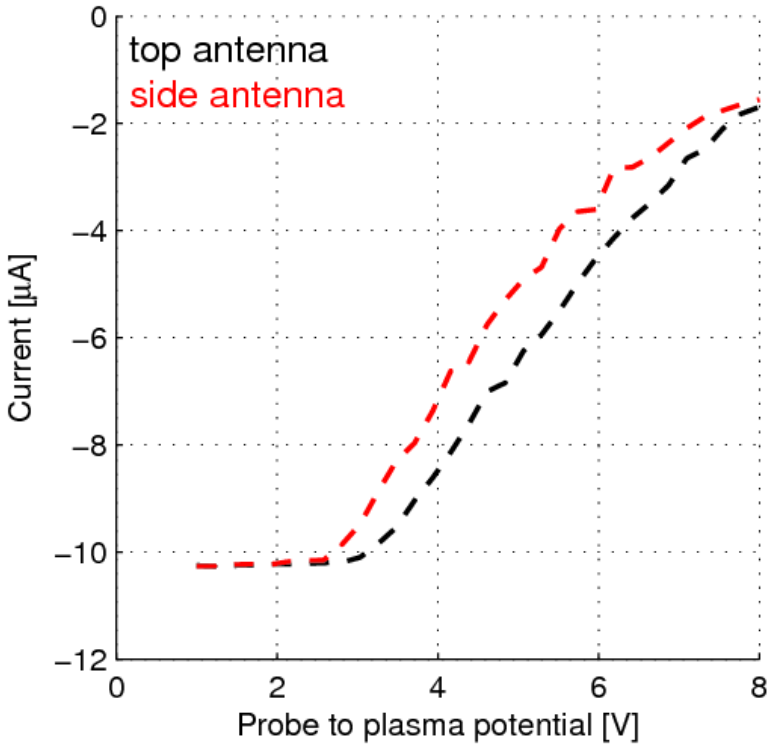

Figure 3 Voltage-current relationship from numerical simulations.

2.3.1.3 Calibration Mode

The BIAS calibration is performed in two steps. At first the antennas are disconnected and the bias current is disconnected so that the instruments internal offsets are determined and secondly the bias current is reconnected and the actual bias current vs. set current is obtained. Calibrations are usually done on a weekly to monthly basis.

2.3.2 Hardware Description

The BIAS comprises a main electronics board located in the MEB and three LF BIAS frontends located in the preamplifier boxes close to the antenna root. A full description of the BIAS design is given in [RD5].

Figure 4 Figure Deleted (BIAS Principle Block Diagram). See [RD5].

2.3.2.1 LF BIAS Frontend

High impedance and low noise LF BIAS frontends are required to detect the low plasma emission levels that are expected in the solar wind. To make a high quality measurement in the wide frequency range from DC up to tens of MHz, the signal from the antennas is split into LF and HF parts that are amplified separately and which later feed the LF and HF analysis parts of the RPW instrument. A wide input dynamic range and a good linearity are needed to make accurate measurements at high frequencies, such as quasi-thermal noise measurements, plasma wave polarization and dynamics, wave particle interactions. Figure 6 (yellow part) shows the principle of the LF BIAS Frontend.

For the highest quality signal, the LF BIAS frontend is located as close as possible to the antenna, inside the thermally isolated box at the root of the stiff antenna boom.

2.3.2.2 BIAS Unit

The probe potential is determined by the bias current (i_{BIAS}) feeding the probes. The probe reaches such a potential that the difference between the plasma current (electrons hitting the probe) and the current due to photoelectrons (electrons leaving the probe) equals the bias current. Usually the bias current is chosen such that the probe reaches a potential that is close to the local plasma potential and the photoelectron current dominates over plasma current (current direction being away from the probe). A positive feedback link, made out of a resistor and a voltage source, across the near unity gain input amplifier forms a current generator feeding the bias current to the antenna. The positive feedback loop gain must be below one for all operational frequencies to avoid oscillations and/or saturation. A simplified schematic diagram illustrating the circuit's principal functions is presented in Figure 5. The bias current setting is under software control.

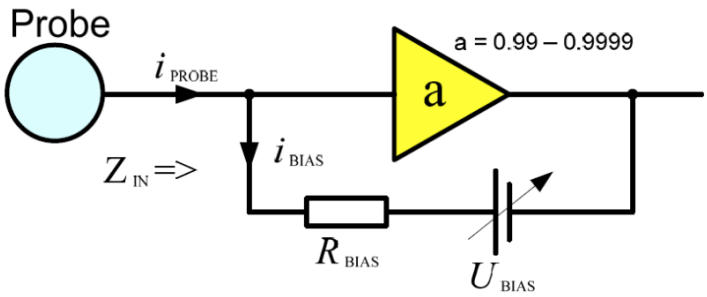

Figure 5 Principle of ANT Current Biasing.

With a gain ideally very close to one, the voltage drop across R_{BIAS} must be equal to the applied U_{BIAS} in magnitude. As the input impedance is high (Gohm) the major part of the current through R_{BIAS} will flow through the probe. The current generated is then ideally $i_{BIAS} = U_{BIAS}/R_{BIAS}$ and the input impedance, seen from the probe, is $Z_{IN} = R_{BIAS}/(1 - \alpha(f))$.

In non-ideal conditions the input offset voltage of the amplifier and the bias current errors need to be accounted for. At launch those errors are small, in the order of 10mV that gives systematic offsets in E-field measurements in the order of 1mV/m. With time, due to radiation, the probe potential errors can drift up to 50mV at the end of the mission, corresponding to systematic offsets in the electric field in the order of 5mV/m. These systematic offsets change on slow time scales and therefore they can be calibrated using particle and magnetic field instrument data (comparing to **v** x **B** fields) or only magnetic field data (requiring the Hofmann-Teller velocity on average to point radially away from the Sun).

2.3.2.3 Floating Ground Concept

The E-field amplifier circuitry has to deal with input signals far in excess of the input ranges of available components. The solution is to apply a "floating ground" that follows the signal. While supply voltages are normally referenced to a common ground, the supplies are referenced to this "floating ground", which is actually not floating, but connected to a buffered voltage that follows the signal. In the Solar-Orbiter electronics the principle of "floating ground" is applied in one step. A voltage, which is a low-pass filtered value of the probe input potential, is used as a "floating ground" for the preamplifier, bias circuitry and stub control. This "floating ground" has a range of ±50 V relative to the spacecraft structure. The purpose is to negate the influence of the spacecraft potential, and hold the signal conditioning circuitry near the plasma potential. This also provides a means to monitor the spacecraft potential. Figure 6 illustrates the "floating ground" concept.

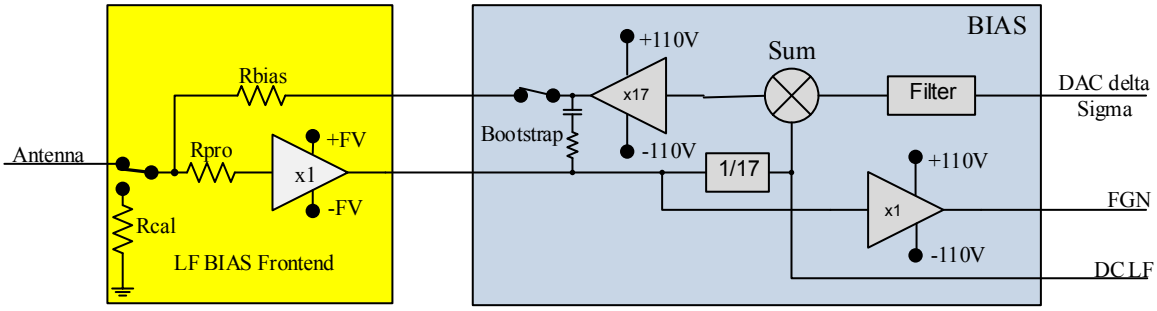

Figure 6 Floating Ground Concept.

The floating supply is limited to 3kHz for power supply reasons. The transition from active current to passive bootstrapping can be set somewhere between 50 and 200Hz. The current value is 100Hz.

2.3.2.4 Analog Outputs to LFR and TDS

Single ended probe DC channels cover the full probe range up to ±50V and are mainly used to determine the satellite potential. For better resolution five differential channels, three DC and two AC, are implemented. All five outputs are sent to LFR, and the three DC channel outputs sent to TDS.

The gain for the DC differential channels is one, with common mode range of ±50V. For the AC channels the gain is set to five or 100, switched via a relay, with a high pass filter at 7Hz, allowing the measurements of electric field range ±100mV/m, assuming 6m efficient distance between antennas (for the expected electric field amplitudes see [RD3]). Each output voltage range is adapted to the receiver input.

For further details of the signals within the BIAS unit, along with the BIAS unit output signals, see [RD5].

Figure 7 Figure Deleted (Output quantities to LFR). See [RD5].

Table 3 Table Deleted (Internal signals within LFR/BIAS unit). See [RD5].

Table 4 Table Deleted (LFR/BIAS unit output signals). See [RD5].

2.3.2.5 Floating Ground DC/DC Converter

The floating ground DC/DC converter provide separate floating ground power supplies for the three LF BIAS frontends and a ±110V supply for the floating ground drivers. The high voltage is referred to ground and is generated by use of diode - capacitance doublers. The floating supplies are insulated from ground and generated by a push pull DC/DC converter running at the RPW dedicated converter frequency. The DC/DC converter is controlled by the FPGA. The transformer has a minimum of two shields between secondary and primary side.

2.3.2.6 FPGA

The following modules are implemented in the FPGA:

- Serial link controller for communication with the DPU
- Control of the three current generator DACs
- Latching relay controllers
- Analog converter for HK
- DC/DC converter clock frequency driver
- Output multiplexer controller

The serial link in/outputs are all buffered by standard LVDS interfaces, before being presented to the DPU. Each module has been used for other projects, however, they have not been configured as for BIAS. A detailed description of the FPGA implementation is given in [RD4].

Figure 8 Figure Deleted (FPGA implementation.) See [RD4].

2.3.2.7 Housekeeping

Analog housekeeping is collected by a first order 16bit Delta Sigma ADC with a 16 bit multiplexer frontend. It is running at 1MHz oversampling and the estimated time for collecting a set of analog BIAS HK is 2 seconds. The modulator comprises a RC network integrator, an amplitude stable reference drive and a center level detector. All parts are controlled by the FPGA that also filters the modulator output and stores the data in a registry. Further details can be found in [RD4] and Section 3.4.4.

Figure 9 Figure Deleted (Principle of analog HK converter.) See [RD4].

2.3.2.8 BIAS DAC

The Bias DAC provides a voltage that is added to the antenna voltage and applied to the bias resistor in order to generate a current. The fourth order delta sigma modulator is implemented in the FPGA and feeds an analog low pass filter and signal conditioner. The low pass filter is set to 400Hz. The modulator is stable and the 16bit accuracy is sufficient to ensure 10 bit operation at end of the mission. Further details can be found in [RD4].

Figure 10 Figure Deleted (BIAS DAC.) See [RD4].

2.3.2.9 Serial Link

The main purpose of the serial link is to have a simple point to point interface for the data/address bus. A very low gate count is needed for the implementation; therefore a space wire link cannot be used. A complete description of the serial link can be found in [RD6].

2.3.3 Software Description

All BIAS software will run in the DPU. It will perform bias settings, bias sweeps, control of relays and output multiplexers.

3 EQUIPMENT REQUIREMENTS

3.1 Functional Requirements

The BIAS unit will satisfy the functional requirements (REQ-RPW-MEB-0101, REQ-RPW-MEB-0102, REQ-RPW-MEB-0106) on the BIAS unit specified in [AD1]. Below are the copies of those requirements from [AD1].

Requirement Number	Requirement Description
REQ-RPW-MEB-0101	The BIAS unit shall permit measurements of the floating potential of all three electric antennas and their differential signal in the DC- 10kHz frequency range.
REQ-RPW-MEB-0102	The BIAS unit shall control the antenna potential by feeding each antenna with a biasing current that can be set in the range ±60μA independently for each antenna.
REQ-RPW-MEB-0106	The BIAS unit shall provide five re-configurable output signals, performed by TC from the DPU, as defined in 3.1.1 [AD1].

3.1.1 Functional Verification Requirements

In addition, following more detailed functional verification requirements shall be satisfied.

Requirement Number	Requirement Description
REQ-RPW-BIA-2100	Functional tests of BIAS shall be carried out with flight-like harness and fully equipped pre-amplifier units in flight configuration.
REQ-RPW-BIA-2101	The stimuli impedances to be used for testing are: 1) 100kOhm‖56pF 2) 1MOhm‖56pF 3) 10MOhm where 56pF is the antenna capacitance to infinity.
REQ-RPW-BIA-2102	During tests the stray capacitance introduced by EGSE must be corrected for, in order to reach the correct base capacitance.
REQ-RPW-BIA-2103	The small signal transfer function shall be measured in frequency range 5Hz-10kHz (minimum), using stimuli impedances as defined in REQ-RPW-BIA-2101 and REQ-RPW-BIA-2102.
REQ-RPW-BIA-2104	The transfer function for all BIAS channels shall be obtained using the stimuli impedances as defined in REQ-RPW-BIA-2101 and REQ-RPW-BIA-2102. For the frequency band near-DC to 10kHz, the worst-case deviation in the transfer function shall: • for amplitude: be less than the sum of $20\log(\frac{C_a}{C_a+C_b})$, the resistive load attenuations and a margin of 3dB, where C_a is the antenna capacitance to infinity and C_b is the antenna base capacitance.

	• for phase: be less than the sum of three poles (each corresponding to -90 degrees) and two zeros (each corresponding to +90 degrees).

Transfer function: The transfer function is composed of several parameters:

1) stimuli used,
2) input characteristic of the preamplifier,
3) efficiency of the bootstrapping of the bias resistor.

At low frequencies bootstrapping of the bias resistor is dominating the transfer function and fully depending of the feed of the bootstrap resistor including flight harness. The low frequencies are also determined by the output resistance of the plasma simulator. At a certain frequency capacitive part of the stimuli and the amplifier input capacitance will dominate the transfer function. This frequency is determined by the stimuli source impedance and the input capacitance load. At low frequencies transfer function should be close to H=1.

3.2 Performance Requirements

The BIAS unit will satisfy the functional requirement REQ-RPW-MEB-0103 on the BIAS unit specified in [AD1]. Below is the copy of that requirement from [AD1].

Requirement Number	Requirement Description
REQ-RPW-MEB-0103	The BIAS unit shall permit measurements of the floating potential of all three electric antennas in the range ±50V.

In addition, the following more detailed performance requirements shall be satisfied.

Requirement Number	Requirement Description
REQ-RPW-BIA-2200	BIAS as a minimum shall satisfy the performance characteristics in Table 2.
REQ-RPW-BIA-2201	Noise shall be measured with BIAS in a full flight configuration in dedicated test setup in EMC clean environment (fully anechoic EMC chamber).
REQ-RPW-BIA-2202	For a verification configuration, which shall at a minimum include the path from the preamplifier input to the output to LFR and TDS, the following shall apply: The Common-Mode Rejection Ratio (CMRR) between two BIAS antenna channels shall be better than -40dB at near DC, and -20dB at 10kHz, assuming that components outside the BIAS board don't degrade the CMRR performance.
REQ-RPW-BIA-2203	Common mode shall be measured: 1) Satisfying REQ-RPW-BIA-2100, REQ-RPW-BIA-2101, REQ-RPW-BIA-2102 2) frequency range 5Hz-10kHz

Noise: Total noise is composed of input amplifier current and voltage noise, the chain of amplifiers to the BIAS output, the positive feedback gain and plasma impedance in relation to the bias resistor. In addition to electronics noise we have also shot noise due to plasma and photoelectrons. The shot noise is estimated analytically.

Common mode is dependent on mechanic and electronic parameters. Common mode performance in space will be dominated by antenna surface property asymmetries and differences in the spacecraft load of antennas. We expect that common mode due to mechanical asymmetries will exceed the common mode of the electronics. Electronic common noise will be dominated by the input impedance differences in the preamplifiers and the impedance differences caused by the flight harness. Differential amplifier used will have a common mode of -54dB at DC/LF.

3.3 Operational Requirements

The BIAS unit will satisfy the operational requirements (REQ-RPW-MEB-0104, REQ-RPW-MEB-0108) on the BIAS unit specified in [AD1].
REQ-RPW-MEB-0107 [AD1] requirement cannot be satisfied. BIAS is not able to operate relays with power off. It has been replaced by external control.

3.3.1 Functional Modes

Mode	Description
Fixed bias	Normal operation mode used most of the time. The levels of the bias currents will be set separately for each probe. The bias currents will be held at a fixed level but will be changed to different levels (about once per a few weeks) depending on the spacecraft distance from the sun or depending on the calibration results from the bias sweeps.
Bias sweep	Usually performed on an hourly to daily basis. The implementation of the sweep mode is done in the software: there is no additional hardware involved.
Calibration verification mode	The antennas are disconnected so that the instrument internal changes in offsets and bias levels can be determined.

Table 5 BIAS unit functioning modes.

3.3.2 Normal Operations

The BIAS unit is set in fixed bias mode.

3.3.3 Coordination with Other Instruments

BIAS sweeps shall not be performed when TBD.
BIAS “sweep flag” set when BIAS performs sweeps.
LFR (and TDS) informed about MUX settings defining BIAS output signals.

3.3.4 In-flight Calibration Verification

The in-flight calibration verification of the signal path from preamplifier to LFR and TDS will be required to adjust the bias settings of antennas. It is carried out by measuring bias current voltage drop across the resistor on the preamplifier input (selected by relay).

3.3.5 Summary of Operational Requirements

Requirement Number	Requirement Description
REQ-RPW-BIA-2300	Sweeps shall be performed frequently defined by the science need.

REQ-RPW-BIA-2301	The in-flight calibration verification shall be performed whenever needed.

3.4 Data Handling Requirements

3.4.1 Data types

u8 = unsigned 8bit data.
s8 = signed 8bit data.
u16 = unsigned 16bit data.
s16 = signed 16bit data.

3.4.2 Telecommands (WRITE)

There will be no command interpreter in the BIAS instrument. Therefore, a BIAS command needs to be converted in the DPU to a 16bit value and sent to a register in the BIAS FPGA via the serial link. The BIAS Write commands are given below, with the full memory map given in [RD4].

Table 6 Table Deleted (Command register map). See [RD4].

3.4.2.1 Set bias 1

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	0	0	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B

R/W=Write(1)
Address A5:0 = 0x28
Data D15:0 = Bias value (µA) = (s16)B * 100 / 32768

3.4.2.2 Set bias 2

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	0	1	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B

R/W=Write(1)
Address A5:0 = 0x29
Data D15:0 = Bias value (µA) = (s16)B * 100 / 32768

3.4.2.3 Set bias 3

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	1	0	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B

R/W=Write(1)
Address A5:0 = 0x2A
Data D15:0 = Bias value (µA) = (s16)B * 100 / 32768

3.4.2.4 DCDC converter (±100V) (Set mode)

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	E	H	0	0	0	0

R/W=Write(1)
Address A5:0 = 0x2B
Data D15:0 = 0x0030 -> ON
Data D15:0 = 0x0020 -> OFF (default)

*Note D5 has to be set in order to accept value in D4 which is useful to mask unwanted writes.

3.4.2.5 Set multiplexer (Set mode)

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	E	M	M	M

R/W=Write(1)
Address A5:0 = 0x2B
Data D15:0 = 0x0008 -> Multiplexer setting 0 (default)
Data D15:0 = 0x0009 -> Multiplexer setting 1
Data D15:0 = 0x000A -> Multiplexer setting 2
Data D15:0 = 0x000B -> Multiplexer setting 3
Data D15:0 = 0x000C -> Multiplexer setting 4
Data D15:0 = 0x000D -> Multiplexer setting 5
Data D15:0 = 0x000E -> Multiplexer setting 6
Data D15:0 = 0x000F -> Multiplexer setting 7

*Note D3 has to be set in order to accept value in D2:0 which is useful to mask unwanted writes. Multiplexer setting is used in conjunction with “Set relay” differential setting between probe 1-3 or 1-2 if needed.

3.4.2.6 Set relays

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	1	0	0	0	0	a	a	b	b	c	c	d	d	e	e	f	f	g	g

R/W=Write(1)
Address A5:0 = 0x2C
Data D15:0 = 0x0001 -> Bypass probe 1 OFF (default)
Data D15:0 = 0x0002 -> Bypass probe 1 ON
Data D15:0 = 0x0004 -> Bypass probe 2 OFF (default)
Data D15:0 = 0x0008 -> Bypass probe 2 ON
Data D15:0 = 0x0010 -> Bypass probe 3 OFF (default)
Data D15:0 = 0x0020 -> Bypass probe 3 ON
Data D15:0 = 0x0040 -> Differential between probe 1 and 2 (default)

Data D15:0 = 0x0080 -> Differential between probe 1 and 3
Data D15:0 = 0x0100 -> Disable Bias 1 (default)
Data D15:0 = 0x0200 -> Enable Bias 1
Data D15:0 = 0x0400 -> Disable Bias 2 (default)
Data D15:0 = 0x0800 -> Enable Bias 2
Data D15:0 = 0x1000 -> Disable Bias 3 (default)
Data D15:0 = 0x2000 -> Enable Bias 3
Data D15:0 = 0x4000 -> AC differential gain x5 (default)
Data D15:0 = 0x8000 -> AC differential gain x100

Setting a relay to either “ON” or “OFF” (1,0 0,1) is allowed while setting both “ON” and “OFF” (1,1) will end in a random state. Setting several relays at once is allowed. Setting “0” on both bits in a bit pair will keep last relay setting. The command will take 3.5 seconds to complete.

3.4.2.7 Set waveform frequency (Sinus) (Set rfeq)

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	1	0	1	A	A	A	E	E	E	R	R	R	R	R	R	R	R	R	R

R/W=Write(1)
Address A5:0 = 0x2D
Data D15:13 = Amplitude setting 0-7 (see table below for actual amplitudes)
Data D12:10 = Enable waveform on probe 1, 2 and/or 3 in any combination (set to 0 when not used).
Data D9:0 = Frequency (Hz) = R * 6.781684028 (R is unsigned 10bit value)

Amplitude	0	1	2	3	4	5	6	7
Actual value	0x000F	0x001F	0x007F	0x01FF	0x07FF	0x1FFF	0x3FFF	0x7FFF
µA	0.046	0.095	0.388	1.559	6.247	24.997	49.997	99.997

3.4.2.8 Set page address

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	P	P	P	P	P	P	P	P

R/W=Write(1)
Address A3:0 = 0x2E
Data D7:0 = Page address 0x00-0xFF

*Note Page address must be reset to 0x00 when no read/write operations are made to RAM.

3.4.2.9 Set sweep

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	1	1	1	E	0	0	0	0	0	0	0	0	0	0	P	P	P	T	T

R/W=Write(1)

Address A5:0 = 0x2F
Data D15:15 = Trig a sweep when set high
Data D4:2 = Enable sweep on probe 1, 2 and/or 3 else collect time series (at least one probe has to be enabled).
Data D9:0 = Set sweep table. Ramp(0), Triangle(1), Log(2), RAM(3) modifiable table

*Note starting a sweep is done with a write with bit 15 set to "1". The two LSB bits(0 and 1) sets which table to use. There are three permanent ROM(0-2) and one programmable RAM(3) tables to choose from, each with 64 steps. Finally bit 2 if set will enable the sweep on probe 1, bit 3 if set will enable sweep on probe 2 and bit 4 if set will enable sweep on probe 3. A sweep takes about 26 seconds to complete and can be polled in the MODE register bit 11.

3.4.2.10 Write sweep table to RAM (Paged_MW)

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	A	A	A	A	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Write(1)
Address A5:0 = 0x30-0x3F and Page number 0x04-0x07
Data D15:0 = Sweep table data (64 values)

*Note setting Page to 4,5,6,7 and writing the 16 values to each page (on actual address 0x30 to 0x3F) will upload the 64 values to the sweep table RAM.

3.4.3 Telemetry

NA

3.4.4 Monitoring and Housekeeping (READ)

Registers and analogue channels will be mirrored into the HK data.
The DPU reads 16 bit data from the HK registers via the serial link, as identified below. The full memory map is given in RD4.

Table 7 Table Deleted (Housekeeping register map.) See [RD4].

3.4.4.1 BIAS1

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Read(0)
Address A5:0 = 0x00
Data D15:0 = Sampled Bias value from DAC1 (µA) = ((s16)(D ^ 0x8000) – 0x56C0)) * -0.01366459

3.4.4.2 BIAS2

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

0	0	0	0	0	0	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Read(0)
Address A5:0 = 0x01
Data D15:0 = Sampled Bias value from DAC2 (µA) = ((s16)(D ^ 0x8000) – 0x56C0)) * -0.01366459

3.4.4.3 BIAS3

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Read(0)
Address A5:0 = 0x02
Data D15:0 = Sampled Bias value from DAC3 (µA) = ((s16)(D ^ 0x8000) – 0x56C0)) * -0.01366459

3.4.4.4 M1

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Read(0)
Address A5:0 = 0x03
Data D15:0 = Sample from Probe 1 signal (V) = (s16)(D ^ 0x8000) * -0.001283997

3.4.4.5 M2

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Read(0)
Address A5:0 = 0x04
Data D15:0 = Sample from Probe 2 signal (V) = (s16)(D ^ 0x8000) * -0.001283997

3.4.4.6 M3

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Read(0)
Address A5:0 = 0x05
Data D15:0 = Sample from Probe 3 signal (V) = (s16)(D ^ 0x8000) * -0.001283997

3.4.4.7 REF

Address	Data

R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L

R/W=Read(0)
Address A5:0 = 0x06
Data D15:6 = Sample of GND(offset). mV = 0.076293945 * ((s16) (DATA ^ 0x8000) >> 6)
Data D5:0 = Sample of +1.5V. V = 0.037974684 * L

3.4.4.8 TEMP1

Address							Data															
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Read(0)
Address A5:0 = 0x07
Data D15:0 = Temperature probe 1 = (s16)(D ^ 0x8000) * 0.1971925 - 273

3.4.4.9 TEMP2

Address							Data															
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Read(0)
Address A5:0 = 0x08
Data D15:0 = Temperature probe 2 = (s16)(D ^ 0x8000) * 0.1971925 - 273

3.4.4.10 TEMP3

Address							Data															
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Read(0)
Address A5:0 = 0x09
Data D15:0 = Temperature probe 3 = (s16)(D ^ 0x8000) * 0.1971925 - 273

3.4.4.11 TEMP_PCB

Address							Data															
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Read(0)
Address A5:0 = 0x0A
Data D15:0 = PCB Temperature = (s16)(D ^ 0x8000) * 0.1971925 - 273

3.4.4.12 NPHV

Address	Data

R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	1	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L

R/W=Read(0)
Address A5:0 = 0x0B
Data D15:8 = Sample of -100V = (s16)(H ^ 0x80) * 1.094118
Data D7:0 = Sample of +100V = (s16)(L ^ 0x80) * 1.094118

3.4.4.13 REF2

Address							Data															
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Read(0)
Address A5:0 = 0x0C
Data D15:0 = Sample of +2.5V reference voltage = (s16)(D ^ 0x8000) * 9.31793E-5

3.4.4.14 MODE

Address							Data															
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Read(0)
Address A5:0 = 0x0D
Data D15:13 = Version number 0-7
Data D12 = Active serial link
Data D11 = Sweep busy
Data D10:8 = Multiplexer setting
Data D7 = HV enabled (±100V)
Data D6 = Enable BIAS3
Data D5 = Enable BIAS2
Data D4 = Enable BIAS1
Data D3 = Diff probe 1&2(0), Diff probe 1&3(1)
Data D2 = Bypass switch probe3
Data D1 = Bypass switch probe2
Data D0 = Bypass switch probe1

3.4.4.15 STATUS

Address							Data															
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	0	0	0	0	0	C	C	C	C	P	P	P	P	P	P	P	P

R/W=Read(0)
Address A5:0 = 0x0E
Data D15 = AC differential gain x5(0) or x100(1)
Data D11:8 = Command counter (counts number of writes made to BIAS)
Data D7:0 = Current Page

3.4.4.16 DUMMY

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Read(0)
Address A5:0 = 0x0F
Data D15:0 = Last written value to the BIAS instrument from serial link

3.4.4.17 Page_read (diagnostics) (Paged_MR)

Address							Data														
R/W	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	A	A	A	A	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

R/W=Read(0)
Address A5:0 = 0x10-0x1F (page 0x00-0xFF)
Data D15:0 = Data from paged memory

*Note the sweep data can be extracted from FPGA RAM on the following addresses:
Probe 1 data can be read on paged address 64-127 (page 4,5,6,7 reading 16 values on each page from address 0x10 to 0x1F).
Probe 2 data can be read on paged address 128-191 (page 8,9,10,11 reading 16 values on each page from address 0x10 to 0x1F).
Probe 3 data can be read on paged address 192-255 (page 12,13,14,15 reading 16 values on each page from address 0x10 to 0x1F).

3.4.5 Time Distribution

NA

3.4.6 Summary of Data Handling Requirements

Requirement Number	Requirement Description
REQ-RPW-BIA-2403	The DPU unit shall send telecommands to BIAS in accordance with RPW-SYS-MEB-BIA-PLN-00041_IRF BIAS FPGA Development Plan, Table 1, BIAS memory map.
REQ-RPW-BIA-2404	The DPU has to collect and process BIAS HK defined by RPW-SYS-MEB-BIA-PLN-00041_IRF BIAS FPGA Development Plan, Table 1, BIAS memory map.

4 GENERAL INTERFACES REQUIREMENTS

4.1 Instrument Identification and Labelling

The serial number of BIAS is available in the HK data. The labeling and numbering of BIAS circuit board is given in [RD7] and its connectors will be made as defined in [RD8].

4.2 Design Requirements

4.2.1 Lifetime and Maintainability

The BIAS will be designed as described in the EID-A and EID-B [RD1 and RD2].

4.2.2 Fault Tolerance

The BIAS will be designed towards the fulfillment of the maximum reliability defined by RPW in the nominal condition. BIAS has only hard reset causing a default state with no antenna output signals.

4.2.3 Safety Concept

The equipment shall be designed with respect with safety philosophy defined in the RPW EID-B [RD2].

4.2.4 Radiation Tolerances

BIAS will be designed to withstand the effects of radiation stated in EID-A and EID-B [RD1 and RD2]. For not compliant parts BIAS will qualify them to an appropriate radiation tolerance level by TID testing.

4.2.5 Summary of Radiation Requirements

Requirement Number	Requirement Description
REQ-RPW-BIA-3201	BIAS shall provide summary reports on parts radiated tested by IRF.

4.3 Mechanical Interfaces Requirements

4.3.1 Mechanical and Structural Design

4.3.1.1 Instrument Location

The Main Electronics Box (MEB) will provide a mechanical structure for housing BIAS. The BIAS PCB will be arranged vertically and fixed into slots of the MEB structure.

4.3.1.2 Mechanical and Structural Concept

PCBs supporting the electronics are mounted into the MEB chassis using mechanical belts. The equipment belt, made of aluminum alloy is a part of the MEB chassis. The mechanical belts are provided by LESIA.

4.3.1.3 External Configuration Drawings

External Configuration Drawing will be provided by LESIA.

4.3.2 Size and Mass

4.3.2.1 Size Specifications

The BIAS PCB surface area is defined by MEB. The allocated slot size for BIAS is 25mm.

4.3.2.2 Mass Budget

See [RD9].
The LF BIAS frontend mass is included in the preamplifier box. External harness to BIAS is not included in the BIAS mass.

4.3.3 Mechanical Environment

BIAS is designed to withstand the mechanical environment defined in the EID A [RD1].

4.3.4 Structural Analysis

The structural analyses of BIAS will be performed by LESIA for the main electronics board and the LF BIAS frontend.

4.4 Thermal Interfaces Requirements

4.4.1 Thermal Interfaces – Definitions

BIAS is considered a collectively controlled unit mounted internally to the MEB chassis.

4.4.2 Thermal Interfaces – Requirements

See [RD9].

4.4.3 Thermal Interfaces – Hardware

4.4.3.1 Conductive and Radioactive Interface

BIAS thermal interfaces are defined by MEB.

4.4.3.2 Temperature Monitoring

BIAS circuit board temperature is monitored. In addition, on each preamplifier circuit board there will be one temperature sensor.

4.4.4 Mathematical Model

4.4.4.1 Thermal Mathematical Model

A Thermal Mathematical Model (TMM) shall be provided by LESIA for the BIAS main electronics board and for the LF BIAS frontend.

4.4.4.2 Thermal Analysis and Temperature Predictions

The temperature predictions for BIAS will be performed by LESIA.

4.5 Power Interfaces Requirements

BIAS is powered by the Low-Voltages Power Supply (LVPS) and the following low-voltages are used:

- 2.2V
- 3.5V

- ±5V.

The DC/DC converter takes its supply from the ±5V supply, and generates ±110V from the diode capacitance doublers and three ±12V floating supplies from a switch transformer. Further details are given in [RD5].

Figure 11 Figure Deleted (DC/DC converter interface.) See [RD5].

4.5.1 Power Budget

This is the **REFERENCE** table for BIAS power ranges.

Estimated values.

Operating modes	+1.5V	+3.3V	-5V	+5V	+12V	Total mW w/o margin	Margin	Total with margin
Standby	200	250	50	50		**550**	10%	**605**
Average	200	250	365	365		**1180**	10%	**1300**
Peak	200	250	365	740		**1555**	10%	**1710**

Measured values on the EM 7 with Actel flash FPGA.

Operating modes	1.5V+ 3.3V mW	-5V + 5V mW	Total mW
Standby	205 (flash FPGA)	65	**270**
Average 30µA DC	205 (flash FPGA)	550	**755**
Peak 100µA DC	205 (flash FPGA)	700	**905**
Nominal AC	205 (flash FPGA)	TBD	**TBD**
Max AC and DC	205 (flash FPGA)	TBD	**TBD**

Peak duration 15sec.

The only peak power to consider in that time frame, is relay power from +5V and energy stored in capacitors.

To be measured.

4.5.2 Interfaces Design

4.5.2.1 Switch On/Off

The PDU is in charge to switch-on/off the equipment by commands from the DPU.

4.5.2.2 Voltages Fluctuations

As defined by the LVPS and its PDU.

4.5.2.3 Short-Circuit Protection

BIAS is designed to survive instantaneous short-circuits occurring on any power line.

4.5.2.4 In-rush Current

To be measured when BIAS is powered by LVPS and PDU.

4.5.2.5 Initial Electrical Status

The BIAS will be designed to survive intentional or unintentional switch-off in any configuration without degradation of its nominal performance. When powered-up, BIAS will be hardware configured to a default mode with 0 bias within 5sec. This cannot be guaranteed if exposed for an on-off-on sequence shorter than 5 sec. HK will be valid 10sec after power on.

4.5.3 Grounding

Distributed Single Point Grounding (DSPG) is used for BIAS. However, there may be a need for direct grounding to chassis of BIAS if the supplied ground causes EMC problems. Figure 12 shows the grounding of BIAS.

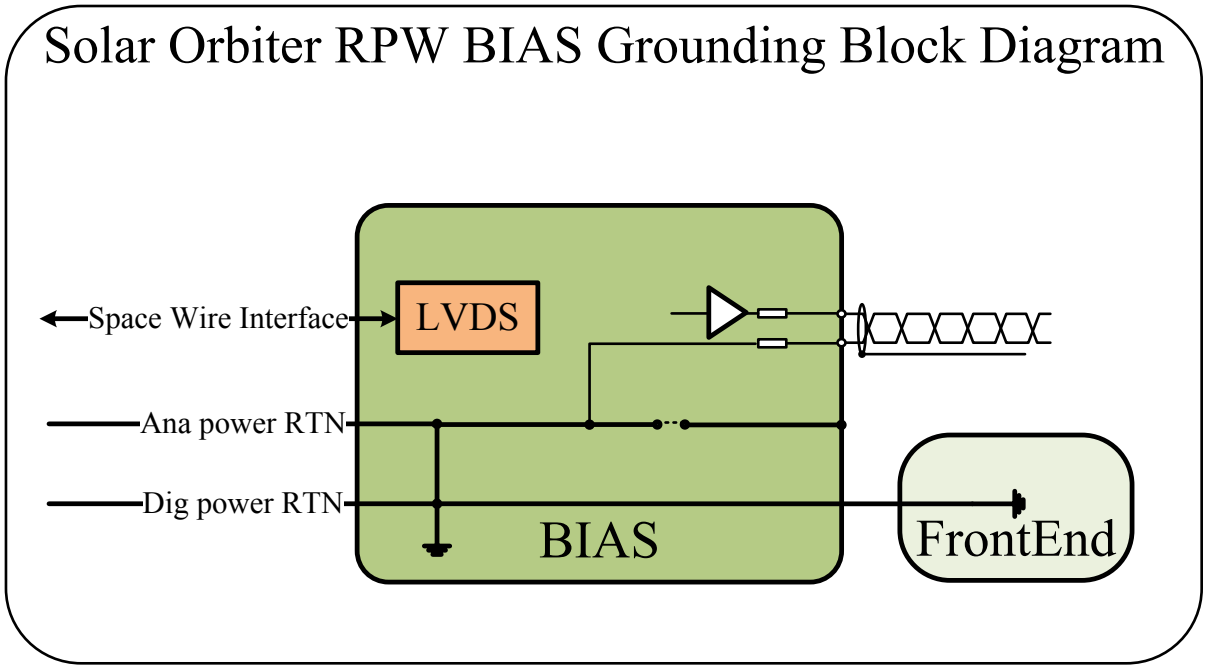

Figure 12 BIAS grounding block diagram diagram.

4.5.4 Summary of Power Interface Requirements

Requirement Number	Requirement Description
REQ-RPW-BIA-3501	The ground impedance (Chassis to BIAS ground) at the open BIAS power connector shall not exceed two times the resistive part of the DC ground resistance at the twentieth harmonics of the common DC/DC converter frequency. (Verified by measurement)
REQ-RPW-BIA-3502	The ground resistance shall be lower than the resistance of two AWG26 in parallel. (Verified by measurement)
REQ-RPW-BIA-3503	The initial stage of BIAS shall be at default stage 5 sec after turn on and HK shall be available 10 sec after turn on.
REQ-RPW-BIA-3504	In case of unacceptable noise levels on the BIAS ground, in reference to satellite chassis, BIAS may be grounded internally to

	chassis.

4.6 Sensor Interface Requirements

4.6.1 Interfaces Diagram

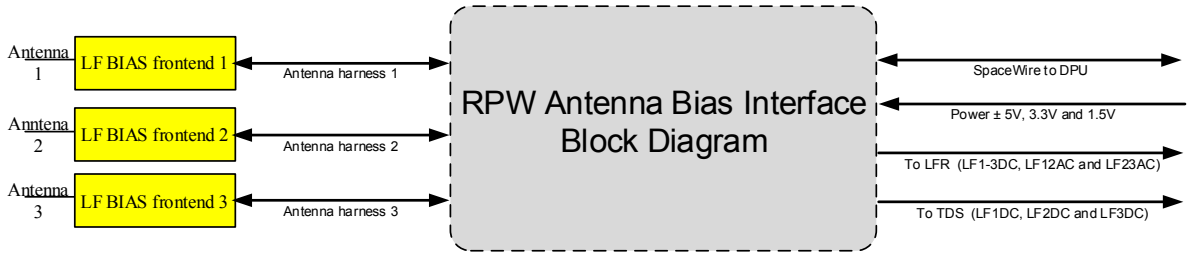

Figure 13 BIAS unit interface diagram.

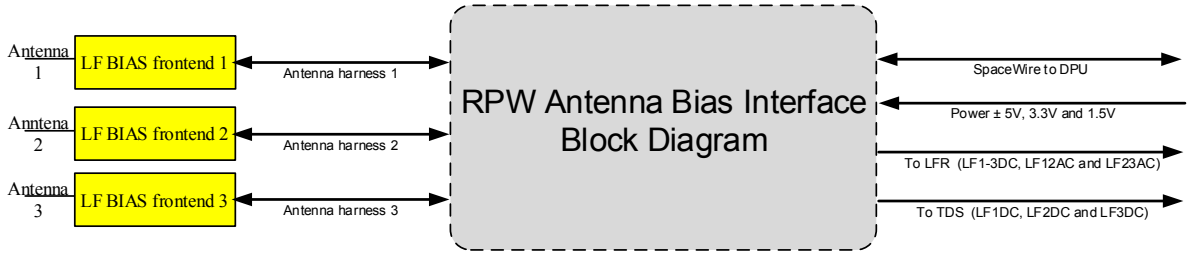

Figure 13 illustrates both the internal and external BIAS sensor interfaces, with outputs to LFR and TDS. BIAS is connected to each antenna through the LF BIAS frontends, located in the RPW preamplifier boxes.

4.6.1.1 Interface to LFR

The LFR interface comprises 5 single-ended outputs with separate ground references. This interface supports a differential receiver input stage, for common mode suppression, on the LFR side. The resistors in the output branches, see Figure 14, are implemented for safety reasons. All available external and internal antenna quantities can be found in [RD5].

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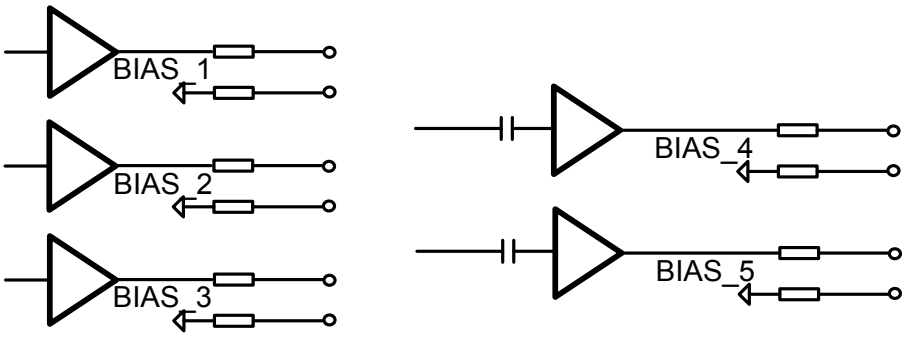

Figure 14 BIAS unit analogue signal interfaces. LFR takes all five outputs, whereas TDS takes outputs BIAS_1, BIAS_2 and BIAS_3 (DC only).

4.6.1.2 Interface to TDS

THE TDS interface comprises the 3 DC single-ended outputs, BIAS_1, BIAS_2 and BIAS_3, using the same configuration as shown in Figure 14. Again further details can be found in [RD5].

4.6.2 Input/Output Stages

4.6.2.1 Input Stages:

BIAS uses positive feedback to create a constant current source for feeding current into the plasma. The current to the plasma determines the BIAS input parameters from DC up to the transition from resistive to capacitive coupled E-fields. In the capacitive region input parameters are determined by the antenna capacitance to the E-field plasma source and the input stage capacitive antenna load to chassis vs. the frequency. Therefore, all BIAS input and transfer parameters are dependent on the antenna to plasma coupling. Those parameters will be obtained during calibration by use of realistic plasma source impedances. The following specifications give the analytic formula for input and transfer parameters using the model in Figure 15 for DC.

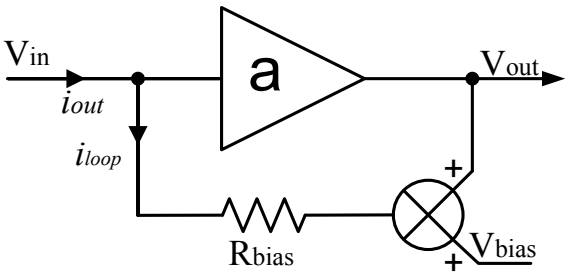

Figure 15 Principle of positive feedback for creating a constant current source.

Input impedance for DC up to the E-field coupling transition is $Z_{in} = \frac{V_{in}}{i_{out}} = \frac{R_{bias}}{1-a}$

in parallel with the amplifier input resistance which in most cases is much higher than Zin . **a** is the positive loop gain and is dependent of the frequency and shall be 0.999 at a minimum for frequencies up to 10kHz and 0.99 for frequencies up to the turn off for the bias resistor bootstrapping at a maximum of 500kHz.

The low frequency transfer function is determined by the plasma voltage source attenuated by Zin * **a** /(Rp+ Zin) where Rp is the plasma source coupling to the antenna.

For high frequencies, were capacitances dominate, the plasma voltage is attenuated by Ca* **a/(**Ca+Cl) where Ca is the plasma source to antenna capacitance and Cl(f) is the antenna load capacitance to satellite chassis.

In the in-between region there will be a one pole transition between the two stages except for the effects caused by the positive feedback.

The input error sources magnification factor is 1/((1/a)-Rp/(Rp+Rbias))

This circuitry is always stable for a<1 and it is stable up to a=1+(Rbias/Rp)

Output current is given by $i_{loop} = i_{out} = \frac{V_{in}}{R_{bias}}(1-a) + \frac{V_{Bias}}{R_{bias}} \overset{a;1}{\approx} \frac{V_{Rbias}}{R_{bias}}$

The output current is unfortunately dependent on Vin and for normal condition this effect can be neglected. However, during sweep it has to be compensated for. The compensation factors will be obtained at calibration and the internal calibration can obtain drifts in that parameter.

The output current will be constant up to 100Hz and thereafter fall off with one pole.

4.6.2.2 Output Stages:

The output from each sensor may individually vary ±50V in reference to the satellite chassis. However, it is not expected to have more than 4V differences between any pair of antennas. Therefore, differential measurements, antenna to antenna, can have a gain of 1 and measurements in reference to satellite ground needs to be attenuated by a factor of 15. To enable AC measurements down to what is stated in Table 2 an AC differential amplifier is introduced with a gain of five, or gain of 100, switched using a relay. The -3dB point for all output drivers should be at 10kHz or higher.
The transfer function from plasma source to LFR output will be obtained at calibration.

4.6.2.3 Conclusions:

All BIAS in/output parameters will be obtained during calibration and used on ground for correction of measured data. Combined they will all be used to verify correct functionality of BIAS as stated in Table 2. This will be reported in the calibration report.

Offsets are not an issue as they can be obtained by internal calibration and can easily be subtracted from measured data at ground.

During integration each subset of electronics will be separately verified by use of specifications given in the parts data sheets. As a reference (requirement) for the verification fundamental analytic formulas for the circuitry will be used.

4.6.3 Harnesses Definition

See [RD8]. The LF BIAS frontend harness configuration is shown in Figure 16.

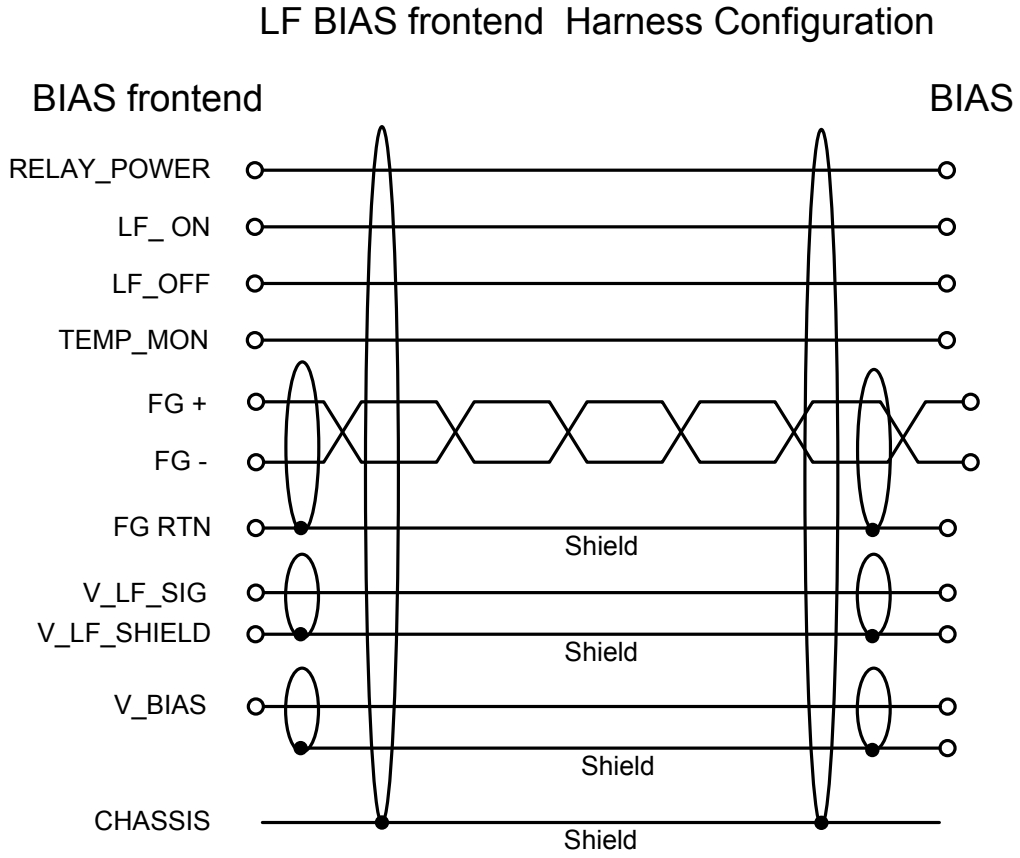

Figure 16 LF BIAS frontend harness configuration.

4.6.4 Connectors and Pins Allocation

In general Micro-D connectors are used for all BIAS interfaces.
Probe harness: 9 pin
Serial Link: 21 pin
Power: 15 pin
Pin allocation: See [RD8]

4.6.5 Summary of Sensors Interfaces Requirements

Requirement Number	Requirement Description
REQ-RPW-BIA-3601	All Input and Output parameters shall be obtained during BIAS calibration and reported in the calibration report.
REQ-RPW-BIA-3602	The calibration results shall show that the requirements in Table 2 are fulfilled by BIAS .

4.7 EMC Requirements

The Bias will fulfill the recommendations on deviations and waivers to the EMC control plan. The EMC requirements are listed in the EID-A [RD1] and EID-B [RD2].

This will be verified at the RPW EMC test.

5 COMMUNICATION INTERFACE REQUIREMENTS

The RPW DPU is the single communication interface with the BIAS unit.

5.1 Interconnection Block Diagram

The BIAS unit shall be connected to the DPU with one bidirectional Serial Link and to the redundant DPU with another bidirectional Serial Link.

5.2 Physical Level

5.2.1 Harnesses Characteristics

The Serial Link cables are normalised SpaceWire cables and will be manufactured according to the scheme given in [RD6].

5.2.2 Connectors and Pins Allocation

The Serial Link connectors shall be micro-miniature D-type (MDM). On the DPU board and unit assemblies, receptacle connectors equipped with female contacts shall be used.

The interface connectors on equipment side shall be 21 contacts with the following pin allocation.

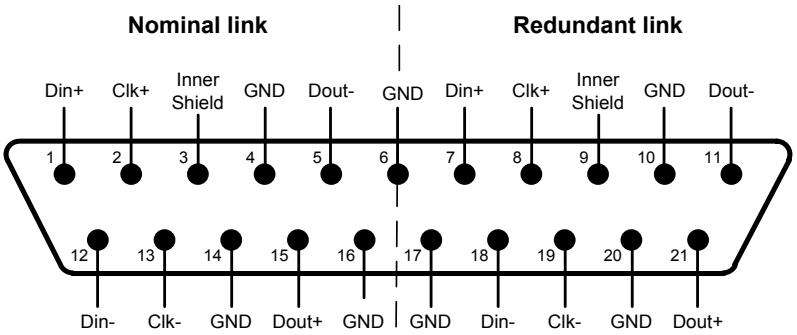

Figure 17 View of the Serial Link front plug on equipment side.

Contact number	Signal name
1	Din+ (Nom.)
2	Clk+ (Nom.)
3	Inner shield
4	GND
5	Dout- (Nom.)
6	GND
7	Din+ (Red.)
8	Clk+ (Red.)
9	Inner shield
10	GND
11	Dout- (Red.)
12	Din- (Nom.)
13	Clk- (Nom.)
14	GND

15	Dout+ (Nom.)
16	GND
17	GND
18	Din- (Red.)
19	Clk- (Red.)
20	GND
21	Dout+ (Red.)

Table 8 Serial Link Contacts Configuration

Note: According to the EMC requirements of the mission, the inner shield of the Serial Link harnesses shall be connected to signal ground of PCB.

5.2.3 Signal Integrity

As well as LVDS signals through cables, the signals transmitted across PCB shall be carefully routed and tracked. Only point-to-point connections are supported.

5.2.3.1 Differential impedance

Differential pair signals shall run on a pair of close, parallel PCB tracks with a differential impedance of 100 ±6Ω. This differential impedance can be achieved by adjusting the track thickness, width, separation and height above the ground plane.

5.2.3.2 Difference in track length for a differential pair

To avoid skew between the two parts of the differential signal, the difference in track length between the two signals from a differential pair shall be less than 5 % of the track length and no more than 5 mm.

5.2.3.3 Difference in track length for Data and Strobe

The skew introduced between the Data and Strobe (D and S) signals shall be minimized as specified here. For PCB tracks, skew is controlled by making the tracks all close to the same length.

The difference in track length between the Data and Strobe signals shall be less than 5 % of the track length and no more than 5 mm.

5.3 Signal Level

5.3.1 Low Voltage Differential Signaling (LVDS)

The Serial Link uses low voltage differential signaling (LVDS) as defined in ANSI/TIA/EIA-644. BIAS unit communication interfaces shall be compliant with the LVDS standards.

5.3.2 Over-voltage Protection

All external LVDS interfaces shall be over-voltage protected below the circuit's absolute maximum VCC ratings. The over-voltage protections shall be achieved using pull-up and pull-down resistors on the LVDS receiver side, as illustrated in Figure 18.

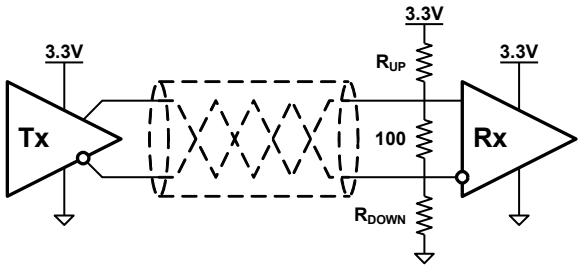

Figure 18 Over-voltage protection.

The pull-up and pull-down resistors shall be nominally as follows:

- R_{UP} = 12kΩ
- R_{DOWN} = 5.6kΩ

5.4 Exchange Level

The exchange level is responsible for making a connection across a link and for managing the flow of data across the link.

5.4.1 Communication Protocol

The communication link with the DPU should be implemented using the IWF Serial Link protocol. A complete description of the serial link can be found in [RD6].

The whole protocol stack is based on a Master/Slave concept of communication according the following approach:

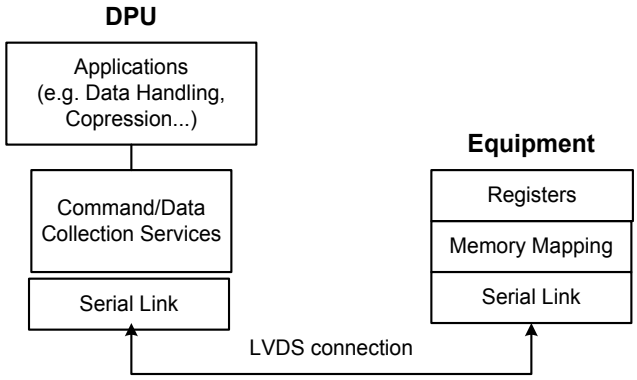

Figure 19 Communication Stack.

5.4.2 Link Timing

5.4.2.1 Link speed

The equipment shall support and keep the link speed within 2MHz +/-1% for both directions.

The DPU will not support changes of the link speed from other units. That means that payloads should use a fixed link speed all along the operations.

5.4.3 System Time Distribution

NA

6 ACRONYMS

ADC	Analogue-to-Digital Converter
CoI	Co-Investigator
DAC	Digital-to-Analogue Converter
DHS	Data Handling System
DPU	Data Processing Unit
EID-A	Experiment Interface Document part A
EID-B	Experiment Interface Document part B
EM	Engineering Model
EMC	Electro Magnetic Compatibility
FM	Flight Model
FPGA	Field Programmable Gate Array
HF	High Frequency
HK	House Keeping
H/W	Hardware
LF	Low Frequency
LFR	Low Frequency Receiver
LVDS	Low Voltage Differential Signaling
LVPS	Low-Voltages Power Supply
MEB	Main Electronics Box
NA	Not Applicable
PAM	Product Assurance Manager
PCB	Printed Circuit Board
PDU	Power Distribution Unit
PI	Principal Investigator
PM	Project Manager
Rad-hard	Radiation-hardened
Rad-tolerant	Radiation-tolerant
RPW	Radio and Plasma Waves (experiment)
S/C	Space Craft
STM	Structural Thermal Model
TBC	To Be Confirmed
TBD	To Be Defined
TC	TeleCommand
TDS	Time Domain Sampler
TID	Total Ionising Dose
TM	TeleMetry
TNR-HFR	Thermal Noise Receiver/High Frequency Receiver